

# NBSG86A

## 2.5V/3.3V SiGe Differential Smart Gate with Output Level Select

The NBSG86A is a multi-function differential Logic Gate which can be configured as an AND/NAND, OR/NOR, XOR/XNOR, or 2:1 MUX. This device is part of the GigaComm™ family of high performance Silicon Germanium products. The device is housed in a 3 x 3 mm 16 pin QFN package.

Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The Output Level Select (OLS) input is used to program the peak-to-peak output amplitude between 0 and 800 mV in five discrete steps.

The NBSG86A employs input default circuitry so that under open input conditions ( $\overline{D}_x$ ,  $\overline{D}_x$ ,  $\overline{VTD}_x$ ,  $\overline{VTD}_x$ , VTSEL) the outputs of the device will remain stable.

### Features

- Maximum Input Clock Frequency > 8 GHz Typical
- Maximum Input Data Rate > 8 Gb/s Typical
- 165 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- Selectable Swing PECL Output with Operating Range:  $V_{CC} = 2.375 \text{ V to } 3.465 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- Selectable Swing NECL Output with NECL Inputs with Operating Range:  $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -2.375 \text{ V to } -3.465 \text{ V}$
- Selectable Output Level (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak-to-Peak Output)
- 50 Ω Internal Input Termination Resistors
- This is a Pb-Free Device



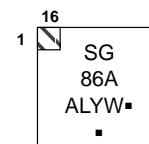
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM\*



QFN16  
MN SUFFIX  
CASE 485G



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

# NBSG86A

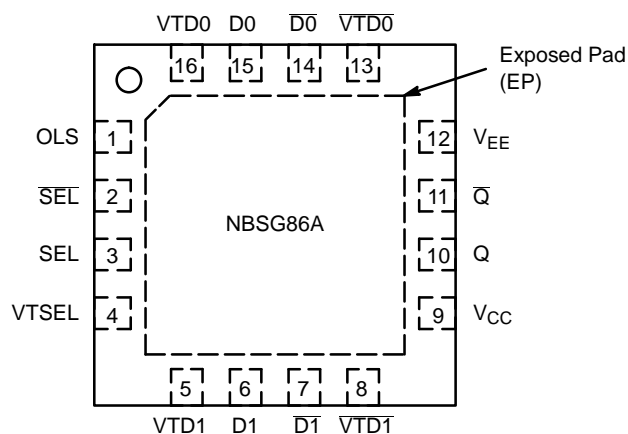


Figure 1. QFN16 Pinout (Top View)

Table 1. Pin Description

Pin	Name	I/O	Description
1	OLS (Note 3)	Input	Input Pin for the Output Level Select (OLS). See Table 2.
2	$\overline{\text{SEL}}$	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Select Logic Input.
3	SEL	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Select Logic Input.
4	VTSEL	–	Common Internal 50 $\Omega$ Termination Pin for SEL/ $\overline{\text{SEL}}$ . See Table 7. (Note 1)
5	VTD1	–	Internal 50 $\Omega$ termination pin. See Table 7. (Note 1)
6	D1	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input 1. Internal 75 k $\Omega$ to $V_{EE}$ .
7	$\overline{\text{D1}}$	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input 1. Internal 75 k $\Omega$ to $V_{EE}$ and 36.5 k $\Omega$ to $V_{CC}$ .
8	$\overline{\text{VTD1}}$	–	Internal 50 $\Omega$ Termination Pin. See Table 7. (Note 1)
9	$V_{CC}$	–	Positive Supply Voltage (Note 2)
10	Q	RSECL Output	Noninverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to $V_{TT} = V_{CC} - 2 \text{ V}$ .
11	$\overline{\text{Q}}$	RSECL Output	Inverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to $V_{TT} = V_{CC} - 2 \text{ V}$
12	$V_{EE}$	–	Negative Supply Voltage (Note 2)
13	$\overline{\text{VTD0}}$	–	Internal 50 $\Omega$ Termination Pin. See Table 7. (Note 1)
14	$\overline{\text{D0}}$	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input 0. Internal 75 k $\Omega$ to $V_{EE}$ and 36.5 k $\Omega$ to $V_{CC}$ .
15	D0	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input 0. Internal 75 k $\Omega$ to $V_{EE}$ .
16	VTD0	–	Internal 50 $\Omega$ Termination Pin. See Table 7. (Note 1)
–	EP	–	The Exposed Pad (EP) and the QFN–16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die but may be electrically and thermally connected to $V_{EE}$ on the PC board.

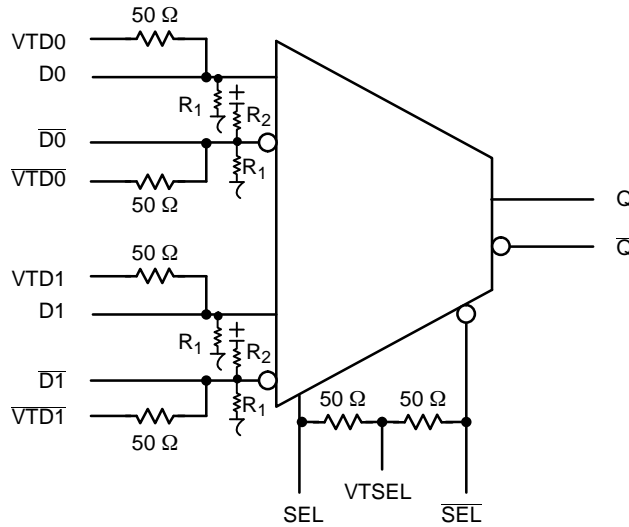
1. In the differential configuration when the input termination pins (VTDx,  $\overline{\text{VTDx}}$ , VTSEL) are connected to a common termination voltage, or left open, and if no signal is applied then the device will be susceptible to self-oscillation.
2. All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.
3. When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0 \text{ V}$ , 2 k $\Omega$  resistor should be connected from OLS pin to  $V_{EE}$ .

# NBSG86A

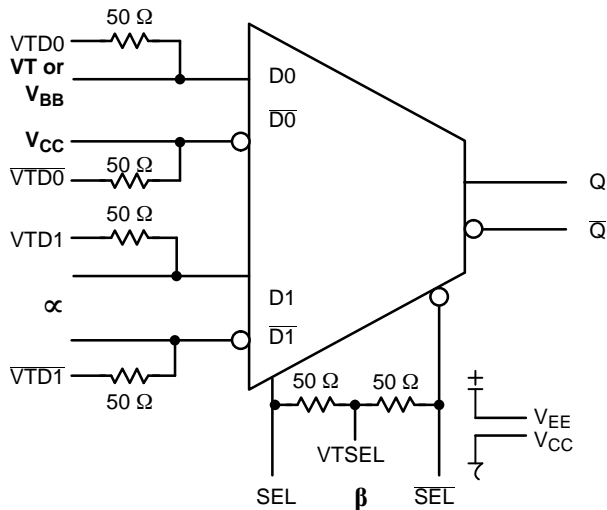
**Table 2. OUTPUT LEVEL SELECT OLS**

OLS	Q/Q VPP	OLS Sensitivity
$V_{CC}$	800 mV	OLS - 75 mV
$V_{CC} - 0.4 V$	200 mV	OLS $\pm$ 150 mV
$V_{CC} - 0.8 V$	600 mV	OLS $\pm$ 100 mV
$V_{CC} - 1.2 V$	0	OLS $\pm$ 75 mV
$V_{EE}$ (Note 4)	400 mV	OLS $\pm$ 100 mV
Float	600 mV	N/A

4. When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0 V$ , 2.0 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .



**Figure 2. Logic Diagram**



**Figure 3. Configuration for AND/NAND Function**

**Table 3. AND/NAND TRUTH TABLE (Note 5)**

	$\alpha$	$\beta$	$\alpha * \beta$
D0	D1	SEL	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

5. D0-bar, D1-bar, SEL are inverse of D0, D1, SEL unless specified otherwise.

# NBSG86A

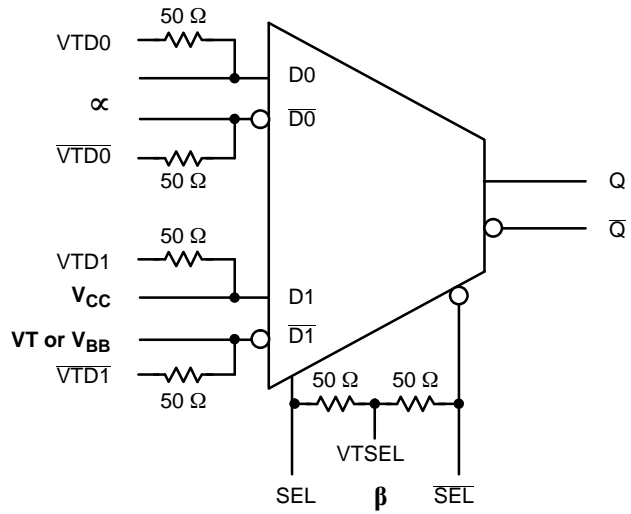


Figure 4. Configuration for OR/NOR Function

Table 4. OR/NOR TRUTH TABLE\*\*

$\alpha$		$\beta$	$\alpha$ or $\beta$
D0	D1	SEL	Q
0	1	0	0
0	1	1	1
1	1	0	1
1	1	1	1

\*\* D0, D1, SEL are inverse of D0, D1, SEL unless specified otherwise.

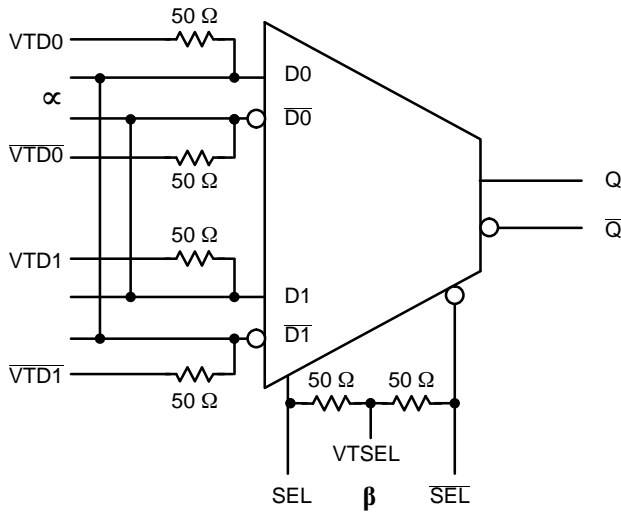


Figure 5. Configuration for XOR/XNOR Function

Table 5. XOR/XNOR TRUTH TABLE\*\*

$\alpha$		$\beta$	$\alpha$ XOR $\beta$
D0	D1	SEL	Q
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0

\*\* D0, D1, SEL are inverse of D0, D1, SEL unless specified otherwise.

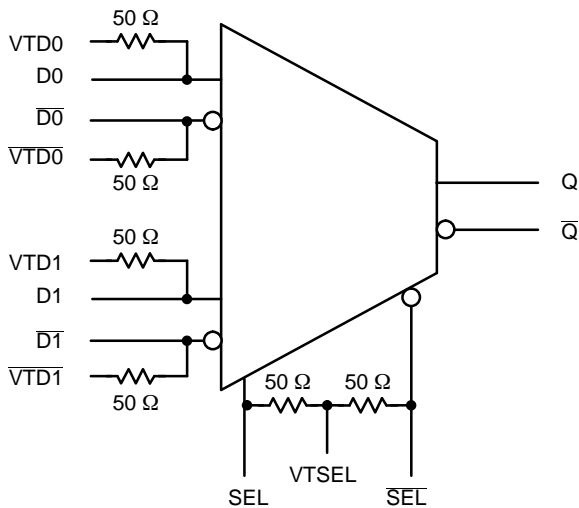


Figure 6. Configuration for 2:1 MUX Function

Table 6. 2:1 MUX TRUTH TABLE\*\*

SEL	Q
1	D1
0	D0

\*\* D0, D1, SEL are inverse of D0, D1, SEL unless specified otherwise.

# NBSG86A

**Table 7. Interfacing Options**

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD0, VTD1, VTSEL and $\overline{\text{VTD0}}$ , $\overline{\text{VTD1}}$ to $V_{CC}$
LVDS	Connect VTD0, VTD1, $\overline{\text{VTD0}}$ and $\overline{\text{VTD1}}$ together. Leave VTSEL open.
AC-COUPLED	Bias VTD0, VTD1, VTSEL and $\overline{\text{VTD0}}$ , $\overline{\text{VTD1}}$ Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage 1.5 V for LVTTTL and $V_{CC}/2$ for LVCMOS inputs.

**Table 8. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistors ( $R_1$ )	75 k $\Omega$
Internal Input Pullup Resistor ( $R_2$ )	37.5 k $\Omega$
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 1 KV > 50 V > 4 KV
Moisture Sensitivity (Note 6)	Pb-Free
	Level 1
Flammability Rating	Oxygen Index: 28 to 34
	UL 94 V-0 @ 0.125 in
Transistor Count	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

6. For additional information, see Application Note AND8003/D.

**Table 9. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	Positive Power Supply	$V_{EE} = 0\text{ V}$		3.6	V
$V_{EE}$	Negative Power Supply	$V_{CC} = 0\text{ V}$		-3.6	V
$V_I$	Positive Input Negative Input	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 -3.6	V V
$V_{INPP}$	Differential Input Voltage $ D_n - \overline{D}_n $ , $ \text{SEL} - \overline{\text{SEL}} $	$V_{CC} - V_{EE} \geq 2.8\text{ V}$ $V_{CC} - V_{EE} < 2.8\text{ V}$		2.8 $ V_{CC} - V_{EE} $	V V
$I_{IN}$	Input Current Through $R_T$ (50 $\Omega$ Resistor)	Static Surge		45 80	mA mA
$I_{out}$	Output Current	Continuous Surge		25 50	mA mA
$T_A$	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 7)	0 lfpm 500 lfpm		41.6 35.2	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	2S2P (Note 7)		4.0	$^{\circ}\text{C}/\text{W}$
$T_{sol}$	Wave Solder	Pb-Free	< 3 sec @ 260 $^{\circ}\text{C}$	265	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

7. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

# NBSG86A

**Table 10. DC CHARACTERISTICS, INPUT WITH LVPECL OUTPUT**  $V_{CC} = 2.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

## POWER SUPPLY CURRENT

$I_{EE}$	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
----------	-------------------------------	----	----	----	----	----	----	----	----	----	----

## LVPECL OUTPUTS (Note 9)

$V_{OH}$	Output HIGH Voltage	1460	1510	1560	1490	1540	1590	1515	1565	1615	mV
$V_{OL}$	Output LOW Voltage										mV
	(OLS = $V_{CC}$ )	555	705	855	595	745	895	625	775	925	
	(OLS = $V_{CC} - 0.4\text{ V}$ )	1235	1295	1385	1270	1330	1420	1295	1355	1445	
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	775	895	1015	810	930	1050	840	960	1080	
	(OLS = $V_{CC} - 1.2\text{ V}$ )	1455	1505	1585	1490	1540	1620	1510	1560	1640	
$V_{OUTPP}$	Output Voltage Amplitude										mV
	(OLS = $V_{CC}$ )	670	800		660	795		655	790		
	(OLS = $V_{CC} - 0.4\text{ V}$ )	125	215		120	210		120	210		
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	510	615		505	610		500	605		
	(OLS = $V_{CC} - 1.2\text{ V}$ )	0	5		0	0		0	5		
	(OLS = $V_{EE}$ )	325	415		320	410		320	410		

## DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 11 & 13) (Note 10)

$V_{IH}$	Input HIGH Voltage (Single-Ended) D, $\bar{D}$ , SEL, $\bar{SEL}$	1200		$V_{CC}$	1200		$V_{CC}$	1200		$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) D, $\bar{D}$ , SEL, $\bar{SEL}$	0		$V_{CC} - 150$	0		$V_{CC} - 150$	0		$V_{CC} - 150$	mV
$V_{th}$	Input Threshold Reference Voltage Range (Note 11)	950		$V_{CC} - 75$	950		$V_{CC} - 75$	950		$V_{CC} - 75$	mV
$V_{ISE}$	Single-Ended Input Voltage ( $V_{IH} - V_{IL}$ )	150		2600	150		2600	150		260	mV

## DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 12 & 14) (Note 12)

$V_{IHD}$	Differential Input HIGH Voltage (D, $\bar{D}$ , SEL, $\bar{SEL}$ )	1200		$V_{CC}$	1200		$V_{CC}$	1200		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage (D, $\bar{D}$ , SEL, $\bar{SEL}$ )	0		$V_{CC} - 75$	0		$V_{CC} - 75$	0		$V_{CC} - 75$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ ) (D, $\bar{D}$ , SEL, $\bar{SEL}$ )	75		2600	75		2600	75		2600	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) (Figure 15)	1200		2500	1200		2500	1200		2500	mV
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ ) D, $\bar{D}$ SEL, $\bar{SEL}$		30 5	100 50		30 5	100 50		30 5	100 50	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ ) D, $\bar{D}$ SEL, $\bar{SEL}$		20 5	100 50		20 5	100 50		20 5	100 50	$\mu\text{A}$

## TERMINATION RESISTORS

$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$
-----------	-------------------------------------	----	----	----	----	----	----	----	----	----	----------

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Input and output parameters vary 1:1 with  $V_{CC}$ .

9. LVPECL outputs loaded with  $50\ \Omega$  to  $V_{CC} - 2\text{ V}$  for proper operation.

10.  $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.

11.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.  $V_{th} = (V_{IH} - V_{IL}) / 2$ .

12.  $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{CMR}$  parameters must be complied with simultaneously.

13.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# NBSG86A

**Table 11. DC CHARACTERISTICS, INPUT WITH LVPECL OUTPUT**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

## POWER SUPPLY CURRENT

$I_{EE}$	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
----------	-------------------------------	----	----	----	----	----	----	----	----	----	----

## LVPECL OUTPUTS (Note 15)

$V_{OH}$	Output HIGH Voltage	2260	2310	2360	2290	2340	2390	2315	2365	2415	mV
$V_{OL}$	Output LOW Voltage										mV
	(OLS = $V_{CC}$ )	1320	1470	1620	1360	1510	1660	1390	1540	1690	
	(OLS = $V_{CC} - 0.4\text{ V}$ )	2030	2090	2180	2065	2125	2215	2090	2150	2240	
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	1550	1670	1790	1585	1705	1825	1615	1735	1855	
	(OLS = $V_{CC} - 1.2\text{ V}$ )	2260	2310	2390	2290	2340	2420	2315	2365	2445	
	** (OLS = $V_{EE}$ )	1785	1875	1995	1820	1910	2030	1850	1940	2060	
$V_{OUTPP}$	Output Amplitude Voltage										mV
	(OLS = $V_{CC}$ )	705	815		695	805		690	800		
	(OLS = $V_{CC} - 0.4\text{ V}$ )	130	220		125	215		125	215		
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	535	640		530	635		525	630		
	(OLS = $V_{CC} - 1.2\text{ V}$ )	0	0		0	0		0	0		
	** (OLS = $V_{EE}$ )	345	435		340	430		335	425		

## DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 11 & 13) (Note 16)

$V_{IH}$	Input HIGH Voltage (Single-Ended) D, $\bar{D}$ , SEL, $\overline{\text{SEL}}$	1200		$V_{CC}$	1200		$V_{CC}$	1200		$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) D, $\bar{D}$ , SEL, $\overline{\text{SEL}}$	0		$V_{CC} - 150$	0		$V_{CC} - 150$	0		$V_{CC} - 150$	mV
$V_{th}$	Input Threshold Reference Voltage Range (Note 17)	950		$V_{CC} - 75$	950		$V_{CC} - 75$	950		$V_{CC} - 75$	mV
$V_{ISE}$	Single-Ended Input Voltage ( $V_{IH} - V_{IL}$ )	150		2600	150		2600	150		2600	mV

## DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 12 & 14) (Note 18)

$V_{IHD}$	Differential Input HIGH Voltage (D, $\bar{D}$ , SEL, $\overline{\text{SEL}}$ )	1200		$V_{CC}$	1200		$V_{CC}$	1200		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage (D, $\bar{D}$ , SEL, $\overline{\text{SEL}}$ )	0		$V_{CC} - 75$	0		$V_{CC} - 75$	0		$V_{CC} - 75$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ ) (D, $\bar{D}$ , SEL, $\overline{\text{SEL}}$ )	75		2600	75		2600	75		2600	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 19) (Figure 19)	1200		3300	1200		3300	1200		3300	mV
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ ) D, $\bar{D}$ SEL, $\overline{\text{SEL}}$		30	100		30	100		30	100	$\mu\text{A}$
			5	50		5	50		5	50	
$I_{IL}$	Input LOW Current (@ $V_{IL}$ ) D, $\bar{D}$ SEL, $\overline{\text{SEL}}$		20	100		20	100		20	100	$\mu\text{A}$
			5	50		5	50		5	50	

## TERMINATION RESISTORS

$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$
-----------	-------------------------------------	----	----	----	----	----	----	----	----	----	----------

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

\*\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a 2 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

14. Input and output parameters vary 1:1 with  $V_{CC}$ .

15. LVPECL outputs loaded with 50  $\Omega$  to  $V_{CC} - 2\text{ V}$  for proper operation.

16.  $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.

17.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.  $V_{th} = (V_{IH} - V_{IL}) / 2$ .

18.  $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{CMR}$  parameters must be complied with simultaneously.

19.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# NBSG86A

**Table 12. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Note 20)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>POWER SUPPLY CURRENT</b>											
$I_{EE}$	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
<b>LVPECL OUTPUTS (Note 21)</b>											
$V_{OH}$	Output HIGH Voltage	-1040	-990	-940	-1010	-960	-910	-985	-935	-885	mV
$V_{OL}$	Output LOW Voltage										mV
	$-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$										
	(OLS = $V_{CC}$ )	-1980	-1830	-1680	-1940	-1790	-1640	-1910	-1760	-1610	
	(OLS = $V_{CC} - 0.4\text{ V}$ )	-1270	-1210	-1120	-1235	-1175	-1085	-1210	-1150	-1060	
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	-1750	-1630	-1510	-1715	-1595	-1475	-1685	-1565	-1445	
	(OLS = $V_{CC} - 1.2\text{ V}$ )	-1040	-990	-910	-1010	-960	-880	-985	-935	-855	
	** (OLS = $V_{EE}$ )	-1515	-1425	-1305	-1480	-1390	-1270	-1450	-1360	-1240	
	$-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$										
	(OLS = $V_{CC}$ )	-1945	-1795	-1645	-1905	-1755	-1605	-1875	-1725	-1575	
	(OLS = $V_{CC} - 0.4\text{ V}$ )	-1265	-1205	-1115	-1230	-1170	-1080	-1205	-1145	-1055	
(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	-1725	-1605	-1485	-1690	-1570	-1450	-1660	-1540	-1420		
(OLS = $V_{CC} - 1.2\text{ V}$ )	-1045	-995	-915	-1010	-960	-880	-990	-940	-860		
(OLS = $V_{EE}$ )	-1495	-1405	-1285	-1460	-1370	-1250	-1435	-1345	-1225		
$V_{OUTPP}$	Output Voltage Amplitude										mV
	$-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$										
	(OLS = $V_{CC}$ )	705	815		695	805		690	800		
	(OLS = $V_{CC} - 0.4\text{ V}$ )	130	220		125	215		125	215		
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	535	640		530	635		525	630		
	(OLS = $V_{CC} - 1.2\text{ V}$ )	0	0		0	0		0	0		
	** (OLS = $V_{EE}$ )	345	435		340	430		335	425		
	$-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$										
	(OLS = $V_{CC}$ )	670	800		660	795		655	790		
	(OLS = $V_{CC} - 0.4\text{ V}$ )	125	215		120	210		120	210		
(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	510	615		505	610		500	605			
(OLS = $V_{CC} - 1.2\text{ V}$ )	0	5		0	0		0	5			
(OLS = $V_{EE}$ )	325	415		320	410		320	410			

**DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 11 & 13) (Note 22)**

$V_{IH}$	Input HIGH Voltage (Single-Ended) D, $\bar{D}$ , SEL, $\bar{SEL}$	$V_{EE} + 1200$		$V_{CC}$	$V_{EE} + 1200$		$V_{CC}$	$V_{EE} + 1200$		$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) D, $\bar{D}$ , SEL, $\bar{SEL}$	$V_{EE}$		$V_{IH} - 150$	$V_{EE}$		$V_{IH} - 150$	$V_{EE}$		$V_{IH} - 150$	mV
$V_{th}$	Input Threshold Reference Voltage Range (Note 23)	$V_{EE} + 950$		$V_{CC} - 75$	$V_{EE} + 950$		$V_{CC} - 75$	$V_{EE} + 950$		$V_{CC} - 75$	mV
$V_{ISE}$	Single-Ended Input Voltage ( $V_{IH} - V_{IL}$ )	150		2600	150		2600	150		2600	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

\*\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a 2 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

20. Input and output parameters vary 1:1 with  $V_{CC}$ .

21. LVPECL outputs loaded with 50  $\Omega$  to  $V_{CC} - 2\text{ V}$  for proper operation.

22.  $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.

23.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.  $V_{th} = (V_{IH} - V_{IL}) / 2$ .

24.  $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{CMR}$  parameters must be complied with simultaneously.

25.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.



# NBSG86A

**Table 12. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Note 20)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY</b> (Figures 12 & 14) (Note 24)											
$V_{IHD}$	Differential Input HIGH Voltage (D, $\bar{D}$ , SEL, $\bar{SEL}$ )	$V_{EE}+1200$		$V_{CC}$	$V_{EE}+1200$		$V_{CC}$	$V_{EE}+1200$		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage (D, $\bar{D}$ , SEL, $\bar{SEL}$ )	$V_{EE}$		$V_{CC} - 75$	$V_{EE}$		$V_{CC} - 75$	$V_{EE}$		$V_{CC} - 75$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ ) (D, $\bar{D}$ , SEL, $\bar{SEL}$ )	75		2600	75		2600	75		2600	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 25) (Figure 15)	$V_{EE}+1200$		0	$V_{EE}+1200$		0	$V_{EE}+1200$		0	mV
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ ) D, $\bar{D}$ SEL, $\bar{SEL}$		30 5	100 50		30 5	100 50		30 5	100 50	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ ) D, $\bar{D}$ SEL, $\bar{SEL}$		20 5	100 50		20 5	100 50		20 5	100 50	$\mu\text{A}$

### TERMINATION RESISTORS

$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

\*\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a 2 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

20. Input and output parameters vary 1:1 with  $V_{CC}$ .

21. LVPECL outputs loaded with 50  $\Omega$  to  $V_{CC} - 2\text{ V}$  for proper operation.

22.  $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.

23.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.  $V_{th} = (V_{IH} - V_{IL}) / 2$ .

24.  $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{CMR}$  parameters must be complied with simultaneously.

25.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# NBSG86A

**Table 13. AC CHARACTERISTICS**

$V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  or  $V_{CC} = 2.375\text{ V}$  to  $3.465\text{ V}$ ;  $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Input Clock Frequency (See Figure 7) (Note 26)	7	8		7	8		7	8		GHz
$V_{OUTPP}$	Output Voltage Amplitude (OLS = $V_{CC}$ ) $f_{in} \leq 7\text{ GHz}$ $f_{in} = 8\text{ GHz}$	590 270	730 440		470 230	720 420		540 180	700 390		mV mV
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential (Figure 16) D/SEL → Q	110	160	210	115	165	215	120	170	220	ps
$t_{SKEW}$	Duty Cycle Skew (Note 27)		5	15		5	15		5	15	ps
$t_{SKEW}$	Channel Skew Q → D/SEL		5	20		5	20		5	20	ps
$t_S$	Set-Up Time (Dx to SEL)	30			30			30			ps
$t_H$	Hold-Up Time (Dx to SEL)	35			35			35			ps
$t_{JITTER}$	RMS Random Clock Jitter (See Figure 7) (Note 29) Peak-to-Peak Data Dependent Jitter (Note 30) $f_{in} \leq 7\text{ GHz}$ $f_{in} \leq 7\text{ Gb/s}$		0.5 12	1.5		0.5 12	1.5		0.5 12	1.5	ps
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 28)	75		2600	75		2600	75		2600	mV
$t_r$ , $t_f$	Output Rise/Fall Times (20% – 80%) (Q, $\bar{Q}$ ) @ 1 GHz $t_r$ $t_f$	30 17	45 35	60 65	30 17	45 35	60 65	30 17	45 35	60 65	ps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

26. Measured using a 500 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ . Input edge rates 40 ps (20% – 80%).

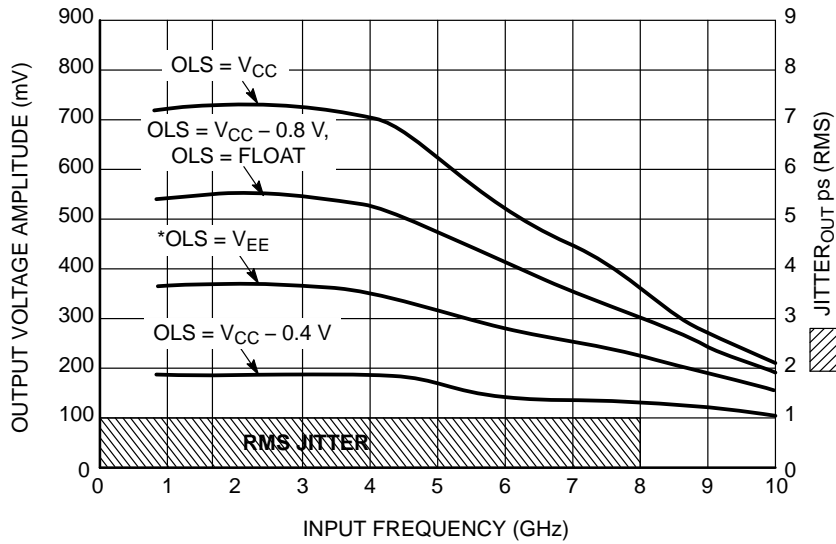
27.  $t_{SKEW} = |t_{PLH} - t_{PHL}|$  for a nominal 50% differential clock input waveform. See Figure 16.

28.  $V_{INPP}$  (max) cannot exceed  $V_{CC} - V_{EE}$ .

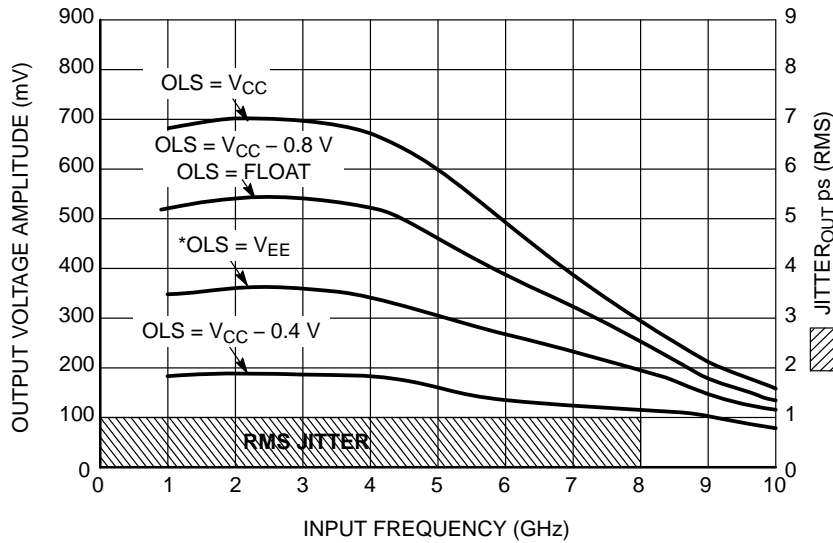
29. Additive RMS jitter with 50% duty cycle clock signal at 7 GHz.

30. Additive Peak-to-Peak data dependent jitter with NRZ PRBS  $2^{31}-1$  data rate at 7 Gb/s.

# NBSG86A



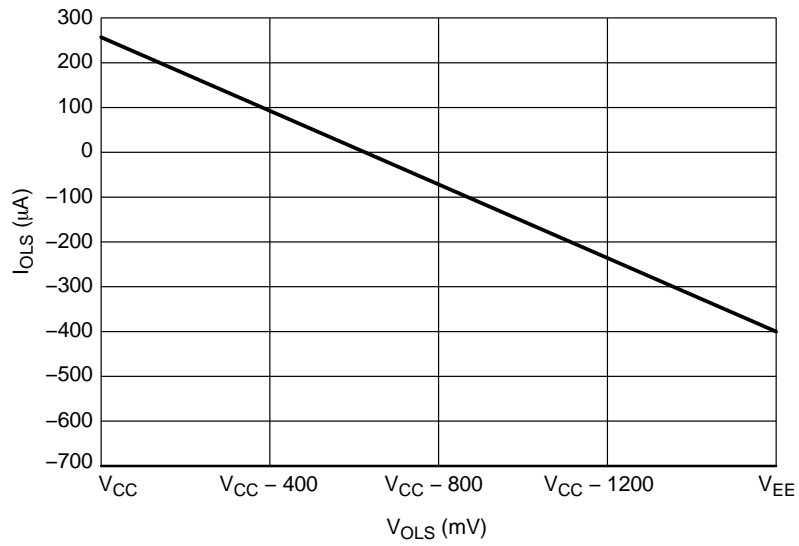
**Figure 7. Output Voltage Amplitude ( $V_{OUTPP}$ ) / RMS Jitter vs. Input Frequency ( $f_{in}$ ) for 2:1 MUX Mode ( $V_{CC} - V_{EE} = 2.5$  V @ 25°C; Repetitive 1010 Input Data Pattern)**



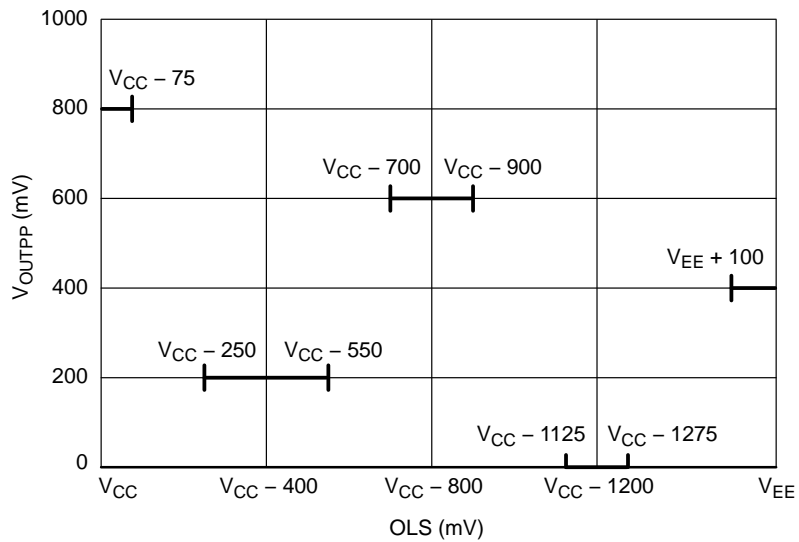
**Figure 8. Output Voltage Amplitude ( $V_{OUTPP}$ ) / RMS Jitter vs. Input Frequency ( $f_{in}$ ) for 2:1 MUX Mode ( $V_{CC} - V_{EE} = 3.3$  V @ 25°C; Repetitive 1010 Input Data Pattern)**

\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0$  V, a 2 k $\Omega$  resistor should be connected from OLS to V<sub>EE</sub>.

# NBSG86A



**Figure 9. Typical OLS Input Current vs. OLS Input Voltage**  
 $(V_{CC} - V_{EE} = 3.3 \text{ V @ } 25^\circ\text{C})$



**Figure 10. OLS Operating Area**

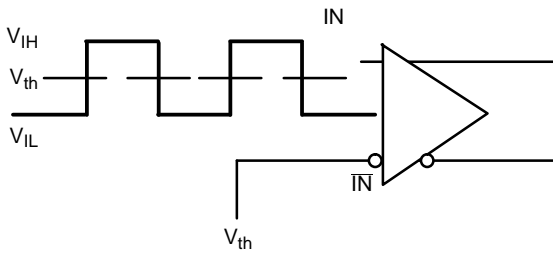


Figure 11. Differential Input Driven Single-Ended

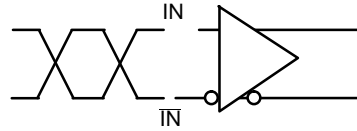


Figure 12. Differential Inputs Driven Differentially

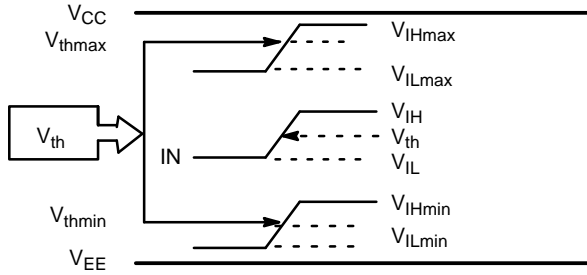


Figure 13.  $V_{th}$  Diagram

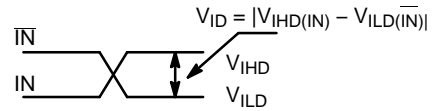


Figure 14. Differential Inputs Driven Differentially

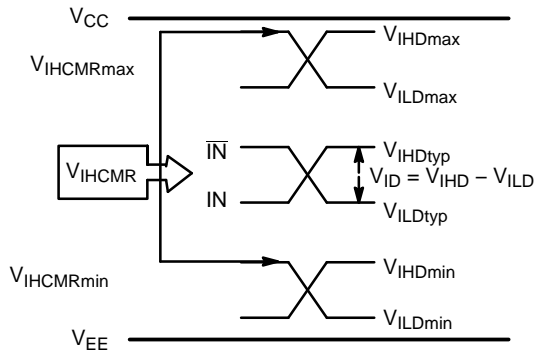


Figure 15.  $V_{IHCMR}$  Diagram

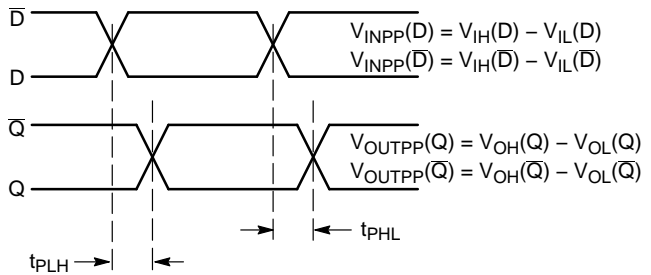


Figure 16. AC Reference Measurement

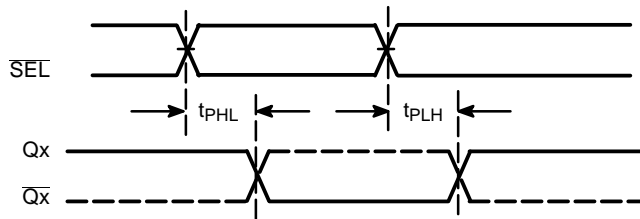


Figure 17. SELx to Qx Timing Diagram

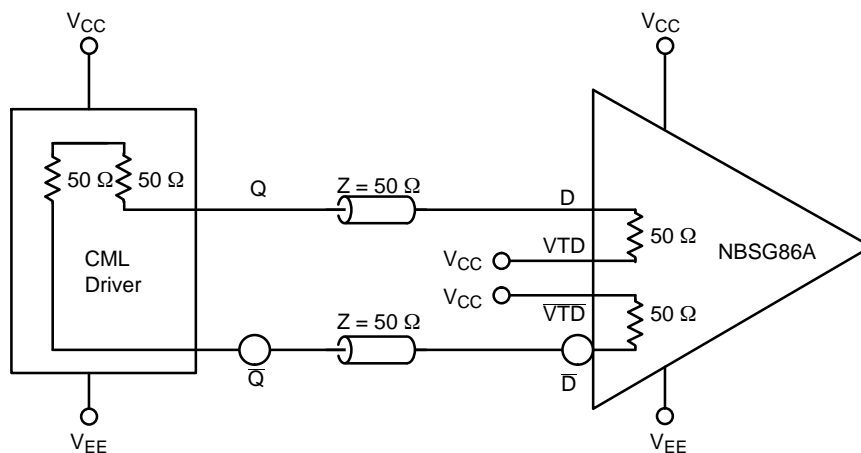
# NBSG86A

## APPLICATION INFORMATION

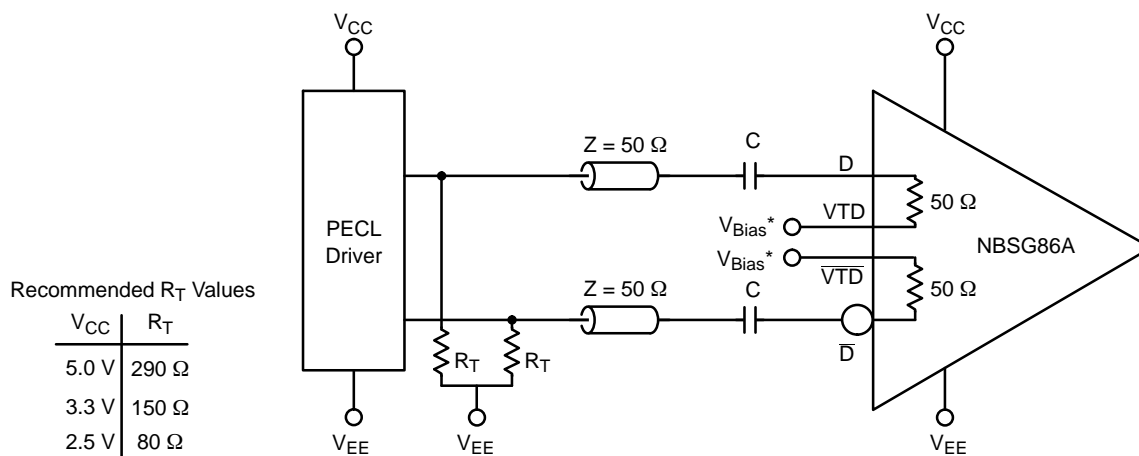
All NBSG86A inputs can accept PECL, CML, LVTTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 75 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from  $V_{CC}$  to 1.2 V. Examples interfaces are illustrated below in a 50  $\Omega$  environment ( $Z = 50 \Omega$ ). For output termination and interface, refer to application note AND8020/D.

**Table 14. INTERFACING OPTIONS**

Interfacing Options	Connections
CML	Connect VTD and $\overline{VTD}$ to $V_{CC}$ (See Figure 18)
LVDS	Connect VTD and $\overline{VTD}$ Together (See Figure 20)
AC-COUPLED	Bias VTD and $\overline{VTD}$ Inputs within Common Mode Range ( $V_{CMR}$ ) (See Figure 19)
RSECL, PECL, NECL	Standard ECL Termination Techniques (See Figure 22)
LVTTTL, LVCMOS	An External Voltage ( $V_{THR}$ ) should be Applied to the Unused Complementary Differential Input. Nominal $V_{THR}$ is 1.5 V for LVTTTL and $V_{CC} / 2$ for LVCMOS Inputs. This Voltage must be within the $V_{THR}$ Specification. (See Figure 21)



**Figure 18. CML Interface**



Recommended  $R_T$  Values

$V_{CC}$	$R_T$
5.0 V	290 $\Omega$
3.3 V	150 $\Omega$
2.5 V	80 $\Omega$

\* $V_{Bias}$  must be within common mode range limits ( $V_{CMR}$ )

**Figure 19. PECL Interface**

# NBSG86A

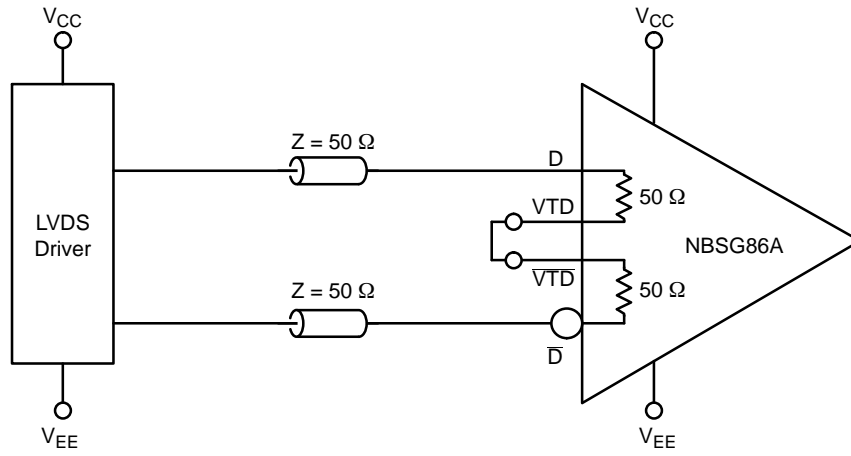


Figure 20. LVDS Interface

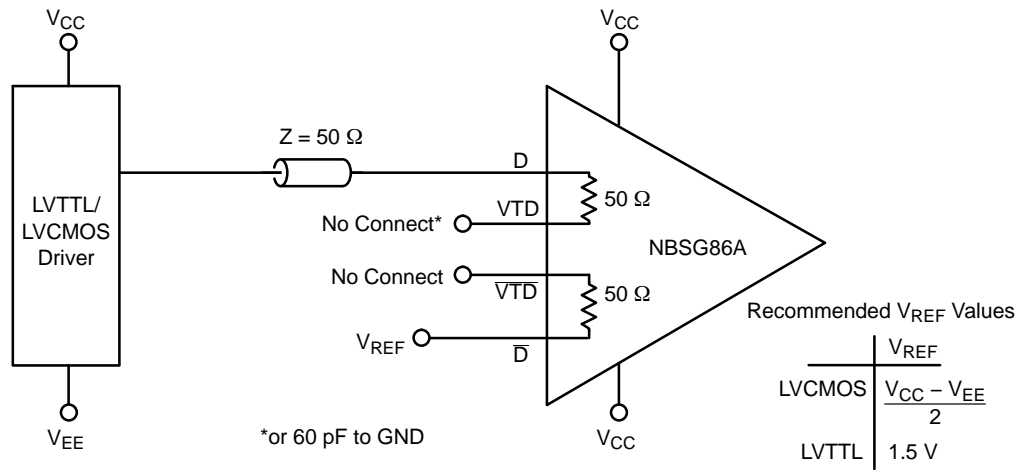


Figure 21. LVC MOS/LVTTL Interface

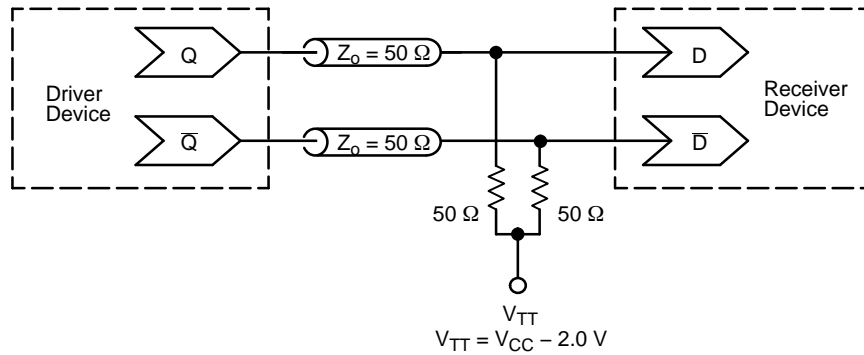


Figure 22. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

# NBSG86A

## ORDERING INFORMATION

Device	Package Type	Shipping†
NBSG86AMNG	QFN16 (Pb-Free / Halide-Free)	123 Units / Rail
NBSG86AMNR2G	QFN16 (Pb-Free / Halide-Free)	3000 / Tape & Reel
NBSG86AMNHTBG	QFN16 (Pb-Free / Halide-Free)	100 / Tape & Reel

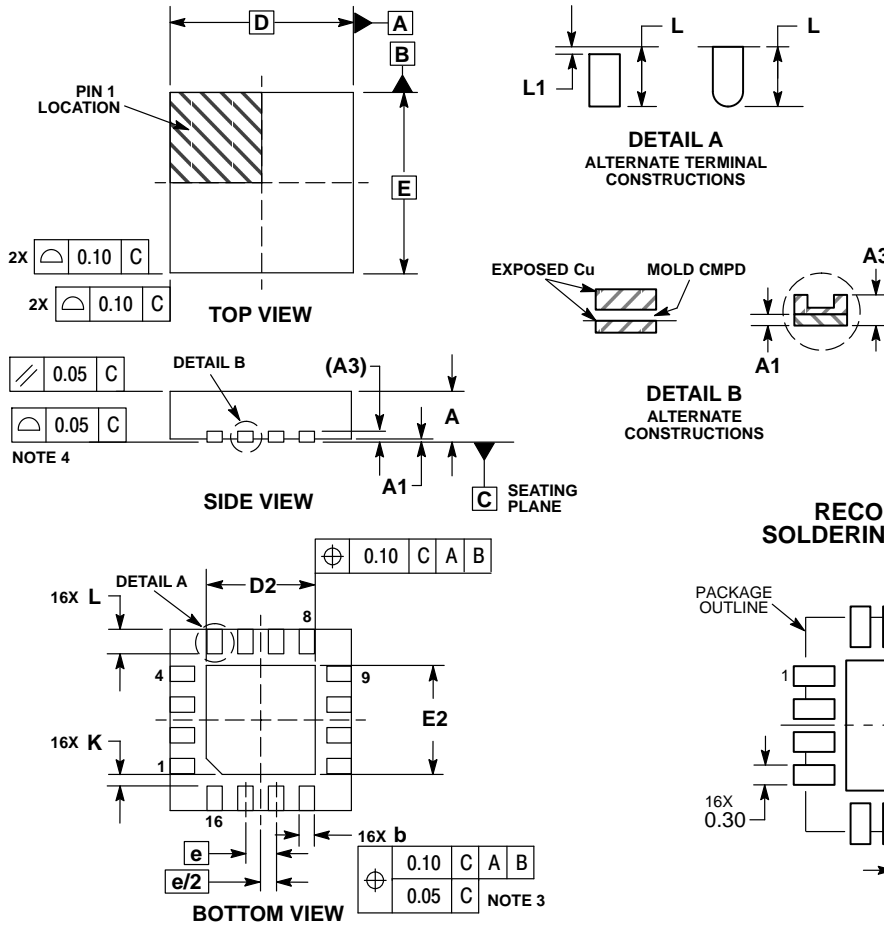
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



# NBSG86A

## PACKAGE DIMENSIONS

QFN16 3x3, 0.5P  
CASE 485G  
ISSUE F



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GigaComm is a trademark of Semiconductor Components Industries, LLC.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative